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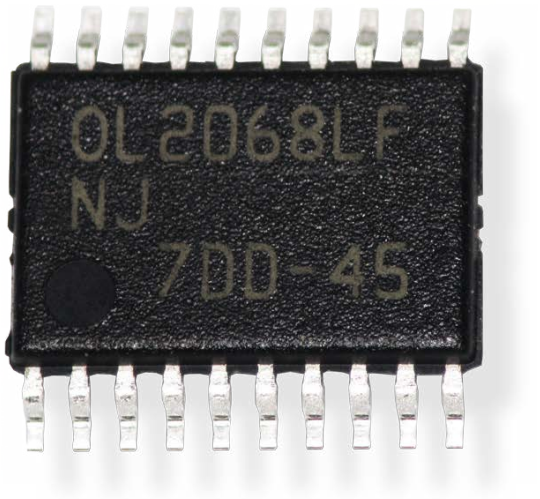
SIMPLY PRECISE



DATA SHEET

OL2068

Industrial 30 Volt 4-Channel Differential Power Line Driver

Index

1. Overview

The OL2068 is an industrial power line driver and contains four identical short circuit proof differential line drivers up to 30 Volts driver supply with a joint enable function. An internal 5 V power supply is used as reference and supply voltage for the circuitry and is able to supply max. 5 mA for external 5 V components like a sensor, or a constant current source for a LED.

The very small outline TSSOP package gives excellent thermal power dissipation, thus the usage in space limited applications is easy.

2. Applications

OL2068 - Industrial 30 Volt 4 Channel Differential Power Line Driver:

- Industrial encoder interfacing
- Industrial sensor interfacing
- Proximity switches
- Industrial controllers
- Light barriers

3. Features

- Ultra small package TSSOP 20
- Max. voltage range from 4.5 V to 36 V
- Short circuit proof tri-state outputs drive up to 120 mA sink / source
- Operating frequency up to 4 MHz
- Integrated voltage reg. with 5 V output
- Dynamic peak current up to 1.5 A
- High impedance CMOS / TTL compatible buffered inputs with hysteresis
- Outputs RS 422 A compatible
- RoHS conform

4. Functional description

The main contents of this new CMOS power line driver are four identical blocks (systems A to D) with each a CMOS/TTL Schmitt Trigger Input and high power differential buffered and inverted outputs. With the low active ENABLE pin it is possible to switch off all eight outputs (high-impedance state), thus this driver can be used in industrial bus systems.

In some rare applications it might be useful to disable the over temperature shutdown. This can be done by setting the ENABLE pin to a level between >7,5 V and <12 V. In this case the whole protection of the IC is disabled! In case of any short circuits or thermal overdrive, the driver might be destroyed! An internal ultra low drop voltage regulator with typical 5.0 V supplies the internal logic to reduce power dissipation. Some applications require additional 5 V (i.e. for an LED driver in an optical encoder). This voltage can be sourced out of the line driver internal voltage regulator (5 mA max.).

The over-temperature protection block is placed in the center of the chip. The thermal shutdown will be activated, when a overload condition (i.e. short circuit) has exceeded the over-temperature detection threshold. In this case automatically all output drivers are switched off and (OL2068) an error signal is activated on a monitor pin. After the chip has cooled down (a few milliseconds) it automatically reactivates all functions and switches the MON output high again. In case the short circuit is still present, it switches off again and the same cycle starts from the beginning. By using this line driver, the field returns of systems, which are accidentally shorted and blown by the end users, are dramatically reduced.

4.1 Power supply

The internal power supply is designed as a voltage regulator with a typical output voltage V_{CCI} = 5.0 V. The minimal voltage drop across the regulator transistors could not be lower than 0.3 V. In order to decouple V_{CCI} it has to be connected to an external capacitor of 100 nF.
The V_{CCI} pin could be used as a reference voltage for LED drivers or is able to supply other external devices like sensors at a maximum current of I_{CCIE} = 5.0 mA. Please keep in mind, that by using this voltage regulator it will generate additional power dissipation = heat.

4.2 Under-voltage reset

If the system is switched on, the status of the line driver is, for a few microseconds, undefined. The same happens, if heavy power supply failures occur. To avoid wrong data transmitted, there is a supply voltage watchdog implemented.

The under-voltage reset block contains a comparator. The voltage V_{CCI} will be always compared with a reference voltage, provided by an internal band gap cell. If after a filter time (t_{FIL}LVR ~ 5 µs) V_{CCI} drops below the typical voltage threshold of 3.5 V the output signal of this block switches off all output drivers to the high-impedance state until minimum 3.6 V are reappearing. In case of such a system fault also the output MON generates an error signal. This (inverted) signal can also be used as a “system ready” signal.

4.3 ESD / EMI

The chip is an ESD sensitive device and should be handled according to guideline EN100015 / part 1 („The Protection of ESD Sensitive Devices„).

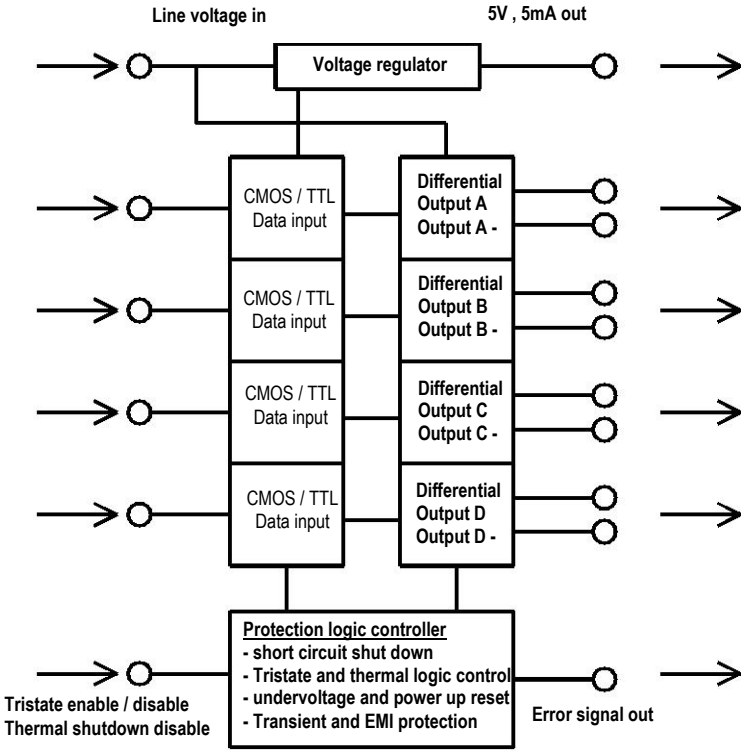
All pins are ESD protected according to ESD standard MIL883, method 3015.7 (human body model). Unused Inputs should be connected to GND, as well as the pin ENABLE in case this function is not used. This will reduce the quiescent supply current.

4.4 Life support clause

The schematics and in general the line drivers are not intended for use in life support appliances, critical components or systems without the express written consent of NUMERIK JENA GmbH. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

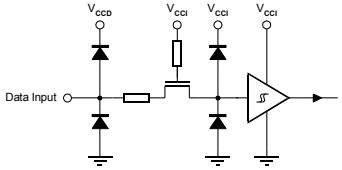
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



4.5 Functional blocks

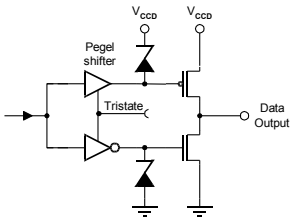
High voltage Data inputs

All Data input pins with Schmitt trigger characteristics on CMOS/TTL level are protected against voltage overshoot up to 30 V. The input circuitry will be powered by an internal low drop voltage regulator.



Push-pull Data outputs

For minimizing cross talk and maintaining the very high switching speed each driver stage has its own level shift pre-driver. Therefore the digital waveform characteristics have a superior frequency response.



4.6 Over-temperature protection

An over-temperature detection and protection is implemented to prevent the output drivers from overheating and being destroyed.

If the temperature increases with growing power dissipation and the junction temperature exceeds the absolute maximum value with typical T_{JOP} ~165 ºC then this condition causes the thermal shutdown by switching off all output drivers to their high-impedance state. After cooling down below the release point the driver will continue his operation. Upgraded power dissipation can be achieved by using a heat link to the board.

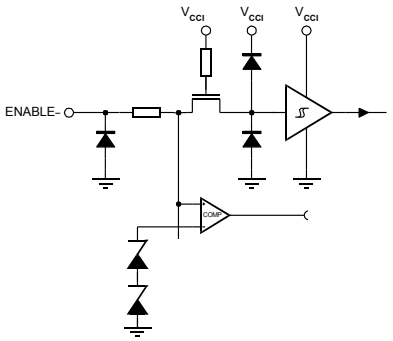
The active over-temperature detection status will be also provided on the MON pin as low level.

4.7 Over temperature disable

The only way to realize this function without a separate pin is the use of a special voltage range on the ENABLE pin.

ENABLE input with temp. disable signal generation

The implementation of one voltage threshold above the valid functional range allows the realization of an additional function. Again - by using this mode the line driver is no longer protected! If there is a voltage >7,5V and <12V applied to the ENABLE pin, the temperature shutdown will be disabled.



5. Technical data

Electrical characteristics

All voltage values are referenced to GND (GND = 0V).
Unless stated otherwise all signals are assumed to be high active.

Table 1 Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Max	Unit
DC supply voltage	V_{CCD}		-0.3	36.0	V
DC input voltage	V_{IN}		-0.3	V_{CC} + 0.3	V
DC input current	I_{IN}			± 10	mA
Output voltage	V_{OUT}		-0.3	V_{CC} + 0.3	V
Driver output current **(see cable model)**	I_{OUT}	pulse peak/average		1500/100	mA
Storage and operating temperature range	T_{STGOP}		-55	+125	°C
Junction temperature	T_J			+150[1]	°C
Lead temperature	T_L	soldering, 10s		+260[2]	°C
Power dissipation: **OL7272LF** SOIC16NB: $R_{th\ j\text{-}a}$ = 111.8 K/W **OL2068LF** TSSOP20: $R_{th\ j\text{-}a}$ = 81.4 K/W	PD	still air, T_A = 85 °C, T_J = 150 °C		 581 798	 mW mW

Table 2 Recommended Operating Conditions

Parameter	Symbol	Condition	Min	Max	Unit
DC supply voltage	V_{CCD}		4.5	30.0	V
DC data input voltage	$V_{IN}D$		0	V_{CCD}	V
DC enable input voltage	$V_{IN}EN$[3]		0	5.5	V
Data output voltage	$V_{OUT}D$		0	V_{CCD}	V
TMON output voltage	$V_{OUT}TM$		0	V_{CCI}	V
Driver output current **(see cable model)**	I_{OUT}[4]			100	mA
Operating ambient temperature range	T_A[5]		-40	+100	ºC
Junction temperature range (lifetime)	T_J		-55	+125	ºC

NOTE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability (e.g. hot carrier degradation).

[1] Look at over-temperature protection Table 3

[2] For surface mounting plastic packages.

[3] Valid for normal function. To disable automatic thermal shutdown, this pin should be set to 7,5 – 12 Volt.

[4] Limited by power dissipation.

[5] Driving capability at elevated temperatures will be limited by total package power dissipation. Special packages up to 125°C can be supplied

Table 3 DC Characteristics (V_{CCD} = 12.0 V, T_A = 25 °C, unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Schmitt trigger inputs section						
Data input hysteresis	$V_{HYS}D$	V_{IL} to V_{IH} and V_{IH} to V_{IL}, ENABLE ≤ 0.8 V	0.2	0.5		V
Data input positive going threshold	$V_{TH+}D$	ENABLE ≤ 0.8 V		1.7	2.4	V
Data input negative going threshold	$V_{TH-}D$	ENABLE ≤ 0.8 V	0.8	1.2		V
Enable input hysteresis	$V_{HYS}EN$	V_{IL} to V_{IH} and V_{IH} to V_{IL},	0.2	0.5		V
Enable input pos. going threshold	$V_{TH+}EN$			1.7	2.4	V
Enable input neg. going threshold	$V_{TH-}EN$		0.8	1.2		V
Data input leakage current - Low	$I_{IL}D$	ENABLE ≤ 0.8 V	-10.0		+10.0	µA
High	$I_{IH}D$	ENABLE ≤ 0.8 V	-10.0		+10.0	µA
Enable input leakage current - Low	$I_{IL}EN$		-10.0		+10.0	µA
High	$I_{IH}EN$		-10.0		+10.0	µA
Push-pull output drive section						
- Low side switch outputs[6]						
Low level output voltage	V_{OLB}	V_{CCD} = 4.75 V, I_{LOAD} = 20mA ENABLE ≤ 0.8 V		0.3	0.5	V
	V_{OLT}	V_{CCD} = 30 V, I_{LOAD} = 30mA, ENABLE ≤ 0.8 V		0.4	0.5	V
Output resistance	R_{DSON}[7]	I_{LOAD} = 30 mA		13	20	Ω
High-impedance output leakage current	I_{OZ}	V_{CCD} = 30.0 V, ENABLE ≥ 2.4 V	-10.0		+10.0	µA
- High side switch outputs[6]						
High level output voltage	V_{OHB}	V_{CCD} = 4.75 V, I_{LOAD} = -20 mA,ENABLE ≤ 0.8V	4.2	V_{CCD} -0.4		V
	V_{OHT}	V_{CCD} = 30V,I_{LOAD} = -30mA, ENABLE ≤ 0.8 V	29.2	V_{CCD} -0.6		V
Output resistance	R_{DSON}[7]	I_{LOAD} = -30mA		20	30	Ω
High-impedance output leakage current	I_{OZ}	V_{CCD} = 30.0 V, ENABLE ≥ 2.4 V	-10.0		+10.0	µA
- MON output[8]						
Low level output voltage	V_{OL}	I_{LOAD} = 2.0 mA			0.4	V
High level output voltage	V_{OH}	I_{LOAD} = -2.0 mA	V_{CCI} -0.8			V
Supply parameters section						
V_{CCD} supply current[9]	I_{DB}(en)	V_{CCD} = 5.0 V, ENABLE ≤ 0.8 V		1.5	5.0	mA
	I_{DT}(en)	V_{CCD} = 30.0 V, ENABLE ≤ 0.8 V		1.5	5.0	mA
	I_{DB}(dis)	V_{CCD} = 5.0 V, ENABLE ≥ 2.4 V		1.5	3.0	mA
	I_{DT}(dis)	V_{CCD} = 30.0 V, ENABLE ≥ 2.4 V		1.5	3.0	mA
Internal supply voltage[10]	V_{CCI}[11]	I_{CCIE} = 5.0 mA	4.5	5.0	5.5	V
Quiescent current	I_{CCQ}[12]	V_{IN} = 2.4 V or 0.8 V		0.2		mA
Current from internal voltage regulator to supply external devices	I_{CCIE}[13]				5.0	mA
Low voltage reset section						
Hysteresis for under-voltage reset	$V_{HYS}LVR$			0.1		V
Under-voltage reset negative going threshold (active)	$V_{TH-}LVR$		3.3	3.5	3.7	V
Under-voltage reset positive going threshold (inactive)	$V_{TH+}LVR$		3.4	3.6	3.8	V
Under-voltage reset filter time	$t_{FIL}LVR$[14]			5		µs
Over-temperature protection section						
Over-temp. operate point (junction)	T_{JOP}			+165	+185	°C
Over-temp. release point (junction)	T_{JRP}		+125	+135		°C

[6] Either the low or high side switch is active at a time.
[7] Values will not be part of the production test but guaranteed by design.
[8] Output MON external driving current up to 4 mA possible – but using this limits the thermal power budget !
[9] Measured without external load on V_{CCI} pin, all outputs open.
[10] For decoupling V_{CCI} please connect this output with a 100nf capacitor to GND
[11] Depends on supply voltage V_{CCD}, V_{CCI} could be not higher than V_{CC} - 0.3 V.
[12] This is measured per input with all other inputs held at V_{CCI} or GND.
[13] Limited by power dissipation, high I_{CCI} current with growing V_{CCD} voltage generates heat, thus the driving limit can be reached earlier
[14] Value will not be part of the production test but guaranteed by design.

Table 4 AC Characteristics (V_{CCD} = 12.0 V, T_A = 25 °C, Cable capacitance 1000pF, unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Disable delay time	t_{OFF}			100	200.0	ns
Enable delay time	t_{ON}			76	600.0	ns
Propagation delay from 50% point of rising edge of input pulse to zero crossing of differential outputs (see Figure 1)	t_{PLH}	V_{CCD} = 5.0 V V_{CCD} = 12.0 V V_{CCD} = 24.0 V C_{LOAD} = 1000 pF		64 74 100	200.0 200.0 330.0	ns ns ns
Propagation delay from 50% point of falling edge of input pulse to zero crossing of differential outputs (see Figure 1)	t_{PHL}	V_{CCD} = 5.0 V V_{CCD} = 12.0 V V_{CCD} = 24.0 V C_{LOAD} = 1000 pF		70 80 100	280.0 280.0 330.0	ns ns ns
Output rise time (see Figure 2)	t_R[15]	V_{CCD} = 5.0 V V_{CCD} = 12.0 V V_{CCD} = 24.0 V C_{LOAD} = 1000 pF		42 110 120	200.0 350.0 380.0	ns ns ns
Output fall time (see Figure 2)	t_F[16]	V_{CCD} = 5.0 V V_{CCD} = 12.0 V V_{CCD} = 24.0 V C_{LOAD} = 1000 pF		32 62 84	200.0 350.0 380.0	ns ns ns

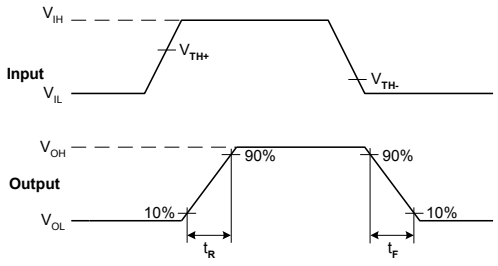


Figure 2
Definition of Output Rise and Fall Time

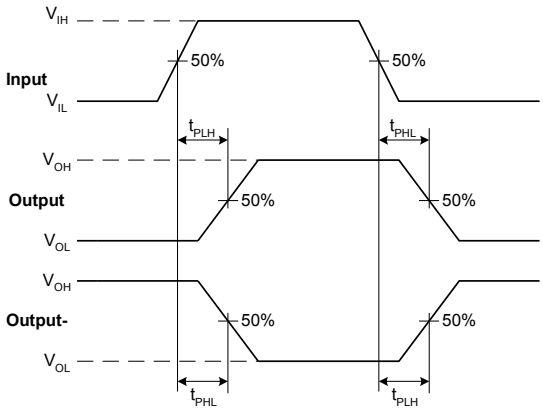


Figure 1
Timing diagram with typical asynchronous propagation delays

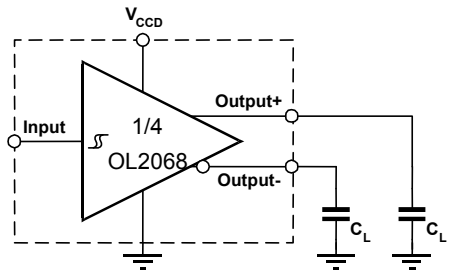
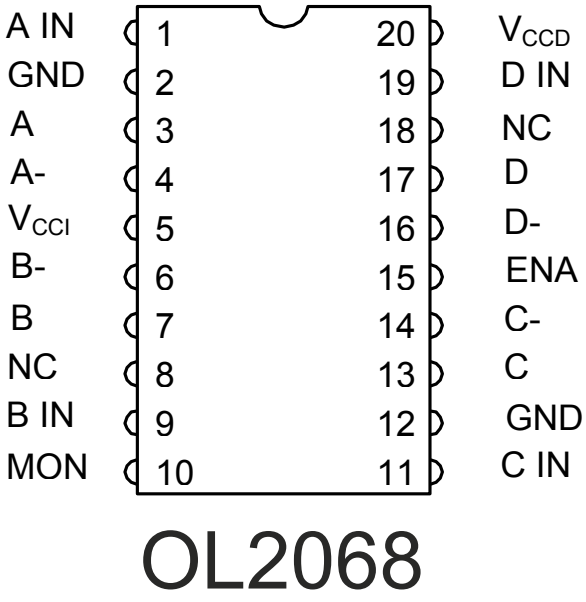
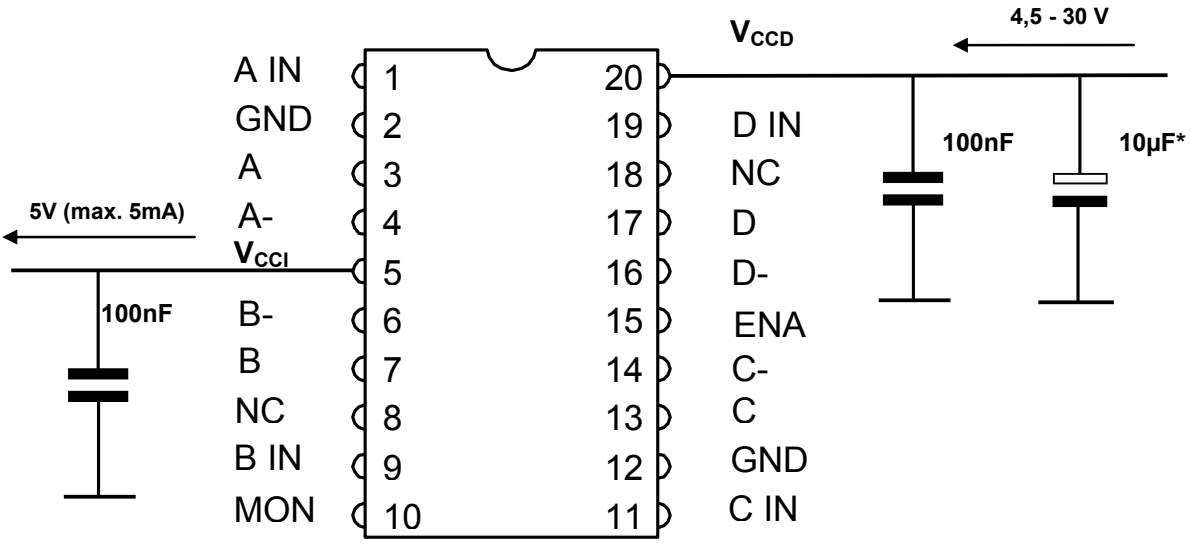


Figure 3
AC Test Circuit
C_L = 1.000pF

[15] Measured from 10% to 90% of the Output signal with a capacitive load on each output pin to ground (see Figure 3).

Pin	Name	I/O Type	Function
1	A IN	INPUT	Input Driver A
2	GND	GROUND	Ground
3	A	OUTPUT	Buffered tri-state Output Driver A
4	A–	OUTPUT	Inverted tri-state Output Driver A
5	V_{CCI}	SUPPLY out	5V internal regulated voltage
6	B–	OUTPUT	Inverted tri-state Output Driver B
7	B	OUTPUT	Buffered tri-state Output Driver B
8	NC		Not connected
9	B IN	INPUT	Input Driver B
10	MON	OUTPUT	Low active Output signal for thermal shut down and under-voltage status
11	C IN	INPUT	Input Driver C
12	GND	GROUND	Ground
13	C	OUTPUT	Buffered tri-state Output Driver C
14	C–	OUTPUT	Inverted tri-state Output Driver C
15	ENA	INPUT	Low active enable Pin for all tri-state Output Drivers
16	D–	OUTPUT	Inverted tri-state Output Driver D
17	D	OUTPUT	Buffered tri-state Output Driver D
18	NC		Not connected
19	D IN	INPUT	Input Driver D
20	V_{CCD}	SUPPLY in	4.5 V to 30 V Driver voltage





Note on OL2068:

The 2 GND pins do not need to be connected to electrical GND simultaneously. One out of them tied to GND is enough. However - for heavy driving of loads it is recommended to tie all four pins to GND.

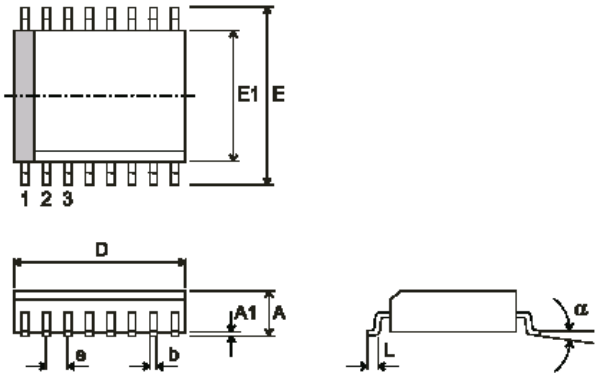
The internal voltage regulator (Pin 5, Vcci) can be used for external loads (5mA max.) as well. Please make sure, that a decoupling capacitor of min. 100nf is connected to Vcci. If, due to heavy loads, the internal voltage supply will be rippled, please increase the capacitor value to stabilize Vcci.

*) This tantalum capacitor will be necessary if supply is not buffered otherwise on the board. The value is application specific and may be decreased on lower supply voltages, lower capacitive loads on the outputs and low supply impedance.

6. Mechanical characteristics

Package dimensions

Symbol	TSSOP20 (173 mil)			Unit
	Min	Typ	Max	
D	6.40(0,25)	-	6.60(0,26)	mm(inch)
E1	4.30(0,17)	-	4.50(0,18)	mm(inch)
E	-	6.40(0,25)	-	mm(inch)
A	-	-	1.20(47)	mm(mils)
A1	0.05(2)	-	0.15(6)	mm(mils)
b	0.19(7)	-	0.30(11)	mm(mils)
e	-	0.65(26)	-	mm(mils)
L	0.50(20)	-	0.75(30)	mm(mils)
α	-	8	-	°



7. Application notes

For differential line driver applications it is recommended to use shielded twisted pair cable. Unfortunately this type of cable is not widely used. A more realistic load circuit is therefore shown in Figure 12. A long cable model is shown in Figure 13.

For better ESD performance it is strongly recommended to use serial resistors of min. 10 Ohms direct behind the output pins.

RL should be adapted to the line impedance to avoid reflections. A typical value is 120 Ohms for twisted pair lines. With higher voltages and frequencies the RL must be increased to not overload the linedriver. Minimum values are listed below. It is also possible to use 2 or more channels in parallel in order to drive higher loads.

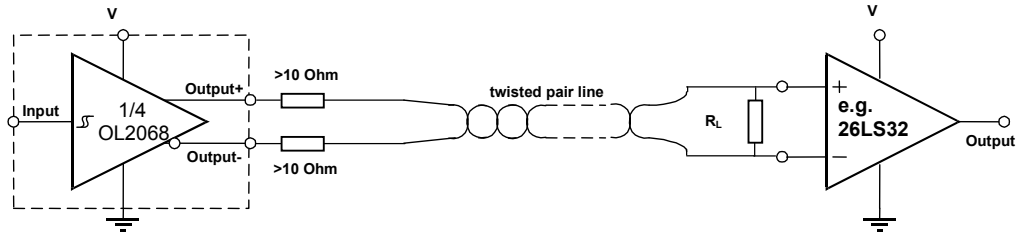
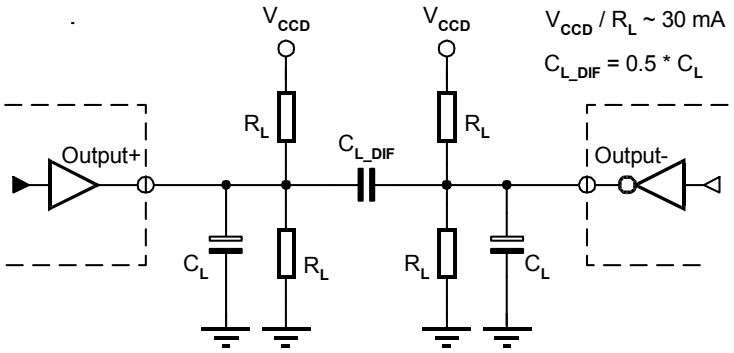


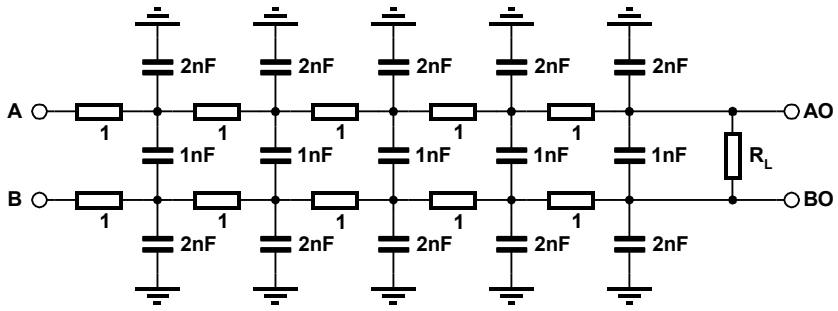
Figure 11 Twisted Pair transmission lines



Parameter RL	Condition	
	V_{CCD}	I_{LOAD}
225 Ω	4.5 V	20 mA
1 kΩ	30 V	30 mA

Figure 12 Load circuit for differential transmission Lines

The variables for Figure 12 to meet the push-pull output drive DC characteristics are:
C_L = 1000 pF, C_{L_DIF} = 500 pF



RL	120 Ω	350 Ω	700 Ω
VCCD	5 V	12 V	24 V

Figure 13 Long cable model (100 m / 330 ft) for differential transmission lines

8. Ordering key

	Batch size (pieces)	Packaging	Ordering-No.
OL2068	72	loose in a tube	626248-01
	1,000	tape & reel	626248-02
	2,500	tape & reel	626248-03

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Technische Änderungen vorbehalten.